MCR-69-369

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FINAL REPORT

FOR

SPACECRAFT MICROMINIATURE PAM DECOMMUTATOR SYSTEM

CONTRACT NAS9-8301

July 1969

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS 77058

Martin Marietta Corporation
Denver, Colorado

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Robert O. Leighou
Program Manager

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FOREWORD

This final report is presented in response to paragraph b of Article XII - Reports of Work of the Contract Schedule for Contract NAS9-8301.

CONTENTS

I. INTRODUCTION AND SUMMARY

The spacecraft microminiature PAM decommutator system has been designed to accept a PAM input signal having the characteristics listed below.

The PAM input signal is positive going and return to zero. Its peak-to-peak amplitude is between 2.5 and 5.0 volts and no excursions below 0 volts dc or +5 volts dc. The normal input signal will have been filtered with a low pass linear phase filter that is 3 db down at 2.3 f_o and has an ultimate roll-off of 18 db per octave. f_o is the data channel rate.

The return-to-zero portion of the input waveform may vary from 0 volts to +2.5 volts but the absolute excursion limits of 0 and +5 volts will be maintained.

A frame sync pulse of 1.5T at the 100% level will occur in the last two channels of each format. The first channel amplitude will be the 0% reference level and will have a pedestal amplitude between 15% and 30% of the peak-to-peak amplitude. The second channel amplitude will be the 100% reference level.

The duty cycle of the PAM input signal may vary between 30% and 70%. The data rate may be any one of four: 30 x 1½, 45 x 2, 90 x 1½ and 90 x 10. The first number is the number of channels per frame and the second is the frame repetition rate per second. This results in channel repetition rates of 45, 90, 112.5 and 900 per second.

Figure I-1 shows a typical waveform.

The PAM decommutator requires a +5 volt signal on the format select line corresponding to the PAM input format. Four format select lines are used for the four formats or data rates.

Using the PAM input signal and the format select signals, the PAM decommutator synchronizes to both the frame rate and channel rate. A positive frame sync level output indicates that synchronization has been achieved. A 4 microsecond output pulse indicates the 1.25T point of the input sync pulse.

The PAM decommutator has two different sets of output signals. The normal output consists of an eight bit parallel address, an eight bit parallel data and a data ready pulse. The requested or computer output consists of an eight bit parallel address, an eight bit parallel data and a data ready flag.

The normal output address and data change for each channel but the requested address changes only for a new request or for an accept. The requested data corresponds to the address and is updated each time the data occurs per frame. The data request pulse and data accept pulse inputs are available to make use of the requested data mode.

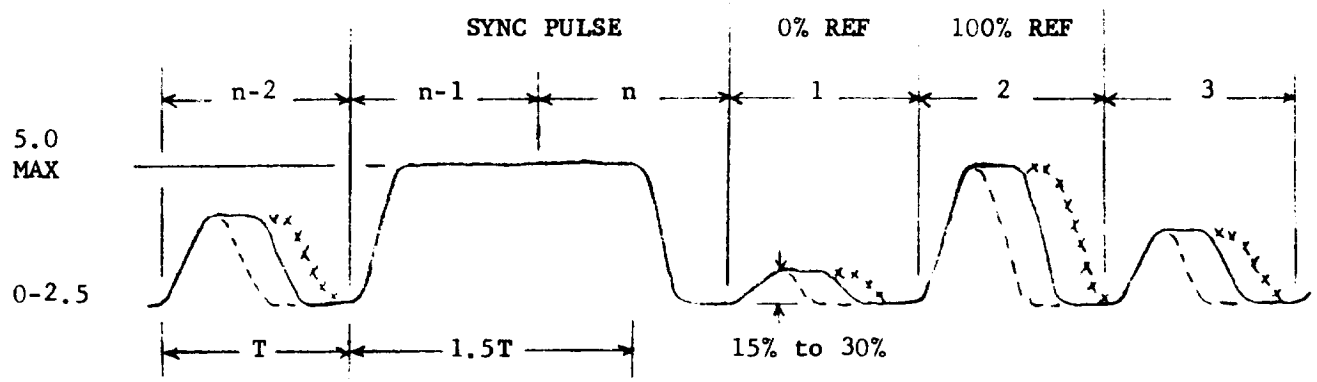

FIGURE I-1, TYPICAL PAM INPUT WAVEFORM

Both of the digital data outputs are normalized with respect to the 0% and 100% references in channels 1 and 2 respectively. A data signal equal to the 0% reference is digitized to 00000001 and a data signal equal to the 100% reference is digitized to 11111110. All data is digitized to an accuracy of $\pm$0.4% of full scale, i.e. the difference between 0% and 100%.

The PAM decommutator was designed, fabricated and tested as required by the latest modification of Exhibit A of the contract. The performance of the PAM decommutator hardware during tests is summarized below:

Temperatures between $0^{o}F$ and $160^{o}F$, altitudes to 200,000 feet, and 100% O_2 atmosphere at 16 psia had practically no effect on the PAM decommutator's operation.

The PAM decommutator did not generate any detectable hazardous gases after 48 hours at 5 psia of 100% O_2.

EMI tests indicated satisfactory tolerance to applied interference including a 10 watt per square meter rf field. EMI tests also indicated satisfactory performance in relation to interference generated by the PAM decommutator.

The acceptance and electrical tests indicated satisfactory performance with the variations of the PAM input signal and the variations of input power.

The general design approach is outlined in Chapter II. A detailed description and the theory of operation are found in the Instruction Manual, MCR-69-321, June 1969.

II. DESIGN APPROACH

A. GENERAL

The basic electrical design approach was to use integrated circuits to the greatest extent possible with the restriction that the components be selected in the following order of precedence:

First - A component with a qualified equivalent from a manufacturer having demonstrated ability to produce a highly reliable component;

Second - A standard qualifiable component from a similar manufacturer;

Third - A selected qualifiable component from a similar manufacturer.

Development of specialized components was avoided.

Low power digital integrated circuits were used to the greatest extent possible. However, in some circuits low power consumption had to be sacrificed for speed, particularly in the A to D converter.

B. DATA CONDITIONING

The data conditioning circuitry provides the following functions:

rf filtering,
high input impedance,
overvoltage protection,
removal of the dc shift,
sampling the data,
disconnecting the input and holding the data value during digitizing,
subtraction of the 0% reference,
addition of the level shift, and
channel pedestal detection.

These requirements are met using integrated circuit operational amplifiers, FET switches and discrete components.

The circuitry consists of rf filters; two balanced input buffer amplifiers; a differential amplifier with two selectable gain constants; a sample-and-hold circuit utilizing FET switches, a storage capacitor and operational amplifier; and a level detector with hysteresis.

C. SYNCHRONIZATION

The synchronization circuitry provides the following functions:

locks the internal clock to the PAM input and maintains sync with:

a. all data channels at 0%,
b. up to 10 consecutive missing pulses,
c. 5% data rate variation per frame, and
d. 20% data rate variation;

recognizes the frame sync input;
generates frame sync pulse and frame sync level outputs;
synchronizes to the four different data rates;
generates timing and control signals;
allows duty cycle variations from 30% to 70%.

These requirements are met using digital and linear integrated circuits, FET switches and some discrete components.

The circuitry consists of a phase locked oscillator that locks to input channel rate divided by two. Two counters are used to determine the relative length of time the PAM input is above the base line and at the baseline. The states of these two counters provide the information to perform most of the functions described above.

D. DIGITIZING

The digitizing circuitry digitizes the output of the sample and hold to eight bits normalized to the 0% and 100% reference channels. These requirements are met using digital and linear integrated circuits, FET switches, a metal grid ladder network and discrete components.

The circuitry consists of a nine-bit sequential approximation analog-to-digital converter complete with an integrated circuit comparator, a gated conversion register, a 0% and 100% storage register, 0% and 100% storage capacitors and associated switches, a reference amplifier with a gain of 255/253 and two buffer amplifiers for the 0% and 100% references. Timing and control for these circuits is supplied by the synchronization circuitry and the A to D (X) counter.

E. DIGITAL INPUT/OUTPUT CIRCUITS

The digital input/output circuitry provides the following functions:

receives an eight bit digital address, a data request pulse and a data accept pulse;
stores the requested data address and data;
stores the normal data address and data from channel to channel;
buffers the following outputs - requested data, requested address, data ready flag, normal data, normal address, normal data ready pulse, frame sync pulse and frame sync level; and
receives the four format select inputs.

The circuitry consists of dual input buffers and threshold bias generators, digital storage registers, and output buffers consisting of an open-collector digital gate with a current limiting FET collector load to plus six volts.

F. POWER SUPPLY

The power supply provides regulated voltages to the circuits as required and both dc and EMI isolation between the input power and the internal circuitry. Discrete components are used in the power supply.

The power supply circuitry consists of an input filter, a switching pre-regulator, a two transformer dc-to-dc converter and output filtering. The outputs are +15, -15, +6 and +5 volts. The +6 volt output has shunt regulation to stabilize the input current requirements for a wide range of output loads.

III. METHODS USED TO MEET SPECIFICATION REQUIREMENTS

This chapter describes briefly the circuitry used to satisfy the requirements of paragraphs 6 and 7 of Exhibit A. The numbers in parenthesis refer to paragraph numbers in Exhibit A.

Input Impedance (6.1) - The 100K ohm minimum input impedance was obtained by using an LM102 buffer amplifier in both the PAM input and its return.

Synchronization (6.2)

a. All channels at 0% - the channel clock detector sensitivity of ±25 millivolts provides detection of 0% channels. Different differentiation time constants are used for Formats A, B and C, and D to maintain this sensitivity;

b. With 10 consecutive missing pulses - the PAM low counter detects missing pulses, switches the phase locked oscillator to the hold mode and provides substitute pulses to maintain proper phasing;

c. With 5% variation per frame - the phase lock loop time constants are such that lock will be maintained;

d. With ±20% variation - the phase lock loop control range of 0 to +10 volts pulls the oscillator more than ±20% from nominal at +5 volts.

Frame Sync (6.3) - The PAM high counter detects the 1.5T sync pulse and controls generation of the frame pulse. The last address logic decodes the address counter and sets the sync window flip flop. The frame pulse transfers the contents of the sync window flip flop to a two stage shift register so that the second frame pulse occurring in the sync window sets the last stage of the shift register which is frame sync level.

Data Rates (6.4) - The four data rates and formats are selected by a +4 to +6 volt signal on any one of four program select lines. These signals are used to initiate the following functions:

a. Select the basic clock division of 16 for the 30 x 1½ rate (Format A), 8 for the 45 x 2 (Format B) and 90 x 1½ (Format C) rates and 1 for the 90 x 10 rate (Format D);

b. Select the basic clock time constant for a nominal 92.16 KHz for formats A and B and 115.2 KHz for formats C and D;

c. Select the integrator time constant for formats A, B and C, and 16 for format D;

d. Select the event start count of 31 for format A, 30 for formats B and C, and 16 for format D;

e. Select the channel clock detector's differentiation time constant for format A, formats B and C, or format D; and

f. Select the last address count of 30 for format A, 45 for format B, and 90 for formats C and D.

Accuracy (6.5) - Conversion of each data channel to an 8 bit binary word with an accuracy of ±0.4% is accomplished by converting and storing the 0% and 100% references to a 9 bit accuracy, by the use of increased gain for signals having a peak-to-peak voltage of less than 3.06 volts, and by feed back techniques to reduce the effects of amplifier drifts, offsets, etc.

Digitizing and Aperture Time (6.6) - These requirements are met by charging the hold capacitor for approximately 100 microseconds just prior to the 0.25T point of each data sample. The sample and hold circuit is disconnected from the signal input just after the 0.25T point and is switched to the hold mode. A to D conversion is then made on this signal. This method prevents any effect from input signal changes during digitizing.

Duty Cycle (6.7) - Any effects due to duty cycle variations from 30% to 70% are avoided by:

a. Providing ±25 millivolt sensitivity for the channel clock detector for positive detection of a 0% signal following a 100% signal with a filtered 70% duty cycle PAM input;

b. Using only the leading edge of each channel in the phase lock loop circuit;

c. Using only the leading edge of each channel for determining the digitizing sequence timing; and

d. Initiating the phase lock loop hold mode after the signal has been at the baseline for 0.875T.

Data Outputs (6.8) - The following data outputs are provided:

Normal Data - an 8 bit binary weighted parallel word that changes for each channel,

Normal Address - an 8 bit binary weighted parallel word with the channel designated as 00000001 being the first channel following the 1.5T sync pulse,

Normal Data Ready Pulse - a 4 microsecond pulse whose leading edge coincides with changing of normal data and normal address and which occurs after digitizing,

Computer or Requested Data - an 8 bit binary weighted parallel word whose contents corresponds to the computer or requested address output which appears or is updated at the leading edge of the normal data ready pulse each time the requested channel occurs,

Computer or Requested Address - the 8 bit binary weighted parallel word designating the requested data that corresponds to the requested address present on the input at the trailing edge of the data request pulse,

Data Ready Flag - an output signal that goes to a logic 1 level at the trailing edge of the normal data ready pulse which occurs during the requested channel thus providing a delay of less than 5 microseconds between the valid data and address and the leading edge of the data ready flag.

The requested data is set to all one's, the requested address to 01111111 (an invalid address) and the data ready flag to logic 0 by the leading edge of the data accepted pulse.

Normalized Data (6.9) - The data is normalized to the 0% reference in channel 1 and the 100% reference in channel 2 by subtracting the 0% reference from each channel signal and digitizing it to a full scale reference equal to 255/253 times the difference between the 0% and 100% references. A 0% data channel is digitized as $\left[\begin{smallmatrix}\text{MSB} & & \text{LSB}\\ 0 & 000000 & 1\end{smallmatrix}\right]_2$ by shifting the sample-and-hold output up 1 bit (1/253 of the full scale reference) during digitizing. A 100% data channel is digitized as $\left[\begin{smallmatrix}\text{MSB} & & \text{LSB}\\ 1 & 111111 & 0\end{smallmatrix}\right]_2$ by the multiplication of difference between the 0% and 100% references by 255/253. The above method of digitizing produces a $[00000000]_2$ output for a signal less than 0% and a $[11111111]_2$ output for a signal more than 100%.

Requested Data Ready Level (6.10) - The data ready flag becomes true at 4.0 $\pm$0.5 microseconds after the requested channel data becomes valid by using the trailing edge of the normal data ready pulse and the output of the address match logic to set the data ready flag. The data ready flag is reset at the leading edge of the data accept pulse.

Test Points (6.11) - The test points are obtained from the following sources thru a 10 Kohm isolation resistor to prevent damage to the unit from grounding the test point (normal operation is continued except for the shorted test point):

Data Input, TP8 - the output of the channel clock amplifier which equals data input times minus 2;

Channel Clock, TP9 - the output of the channel clock detector;

Frame Sync (Level) Indicator, TP2 - the 1 output of the frame sync level flip flop;

Data to Digitizer (Output of S & H), TP10 - the output of the sample-and-hold amplifier;

Output of Comparator, TP7 - the output of a D type flip flop (to remove comparator noise) that controls the successive approximation reset signals;

Digitizing Aperture Time, TP4 - the time from the most significant bit decision to the least significant bit decision obtained by decoding the X counter for X4 or X6;

Normalized 0% Ref, TP11 - the output of the 0% amplifier;
Normalized 100% Ref, TP12 - the output of the full scale amplifier;
Gain State, TP5 - the 1 output of the gain state flip flop - logic 1 for high gain and logic 0 for low gain;
VCO Input, TP13 - the output of the phase lock loop integrator;
Omega Bar, TP1 - the 1 output of U7 in the U counter - a symmetrical waveform approximately 180° out-of-phase with PAM input signal;
Data Sample Interval. TP6 - the gate output that controls the sample-and-hold switching;
+15, TP14 - the +15 volt supply;
-15, TP17 - the -15 volt supply;
+5, TP16 - the +5 volt supply; and
+6, TP15 - the +6 volt supply.

Output Voltage Levels (6.12) - The output voltage levels are: a binary 1 - a saturated FET switch to +6 volts; and a binary 0 - a saturated transistor gate output to ground.

Rise Time (6.13) - The 0.2 microsecond rise time is met by the turn-off of the transistor gate and is typically 0.1 microsecond.

Output Pulses (6.14) - The output pulses have the same output buffer as the output levels. The pulse width is determined by a 9601 one shot having a nominal pulse width of 4.0 microseconds.

Output Impedance (6.15) - The 100 ohm output impedance is obtained by specifying R_{DSS} of the FET's to be less than 100 ohms and by the saturated transistor gate with a 25 ohm output impedance. This will drive the 2 Kohm or greater load as required.

Shortage Protection (6.16) - Normal operation of all logic levels is for a logic 0 output to be obtained by shorting the output to output return. There is, therefore, no effect from an output short.

Operating Temperature Range (6.17) - The PAM decommutator was designed to operate over the temperature range of -30°F to +185°F by using components and proper derating such that they will withstand the internal temperatures resulting from these ambient temperatures. The PAM decommutator operated successfully at the 0°F and 160°F ambient temperatures.

RFI (6.18) - The unit was designed and tested in accordance with NASA IESD 19-3.

RF Filtering (6.19) - Additional RF filtering was utilized to meet and successfully test to these requirements.

Supply Current (6.20) - Minimum supply current was obtained by utilizing low power logic circuits wherever possible.

Warm-up (6.21) - All circuitry is operating within milliseconds of power application with no warm-up, per se, required. There is, however, a possible delay of one to two frames before indication of frame sync to prevent false sync indications.

Signal Overvoltage (6.22) - Signal overvoltage protection is provided by limiting the buffer input voltages to ±15 volts by diodes to the ±15 volt supplies. This voltage is within the input buffer and differential amplifiers capabilities.

Computer Levels (6.23) - The computer input buffers are biased to +3.75 volts and have a tested output at ±0.25 volts from this bias point.

Rise and Fall Times (6.24) - The input buffers will respond to signals from dc to those having rise times in the tens of nanoseconds. Their typical input to output delay is 150 nanoseconds which provides excellent response to signals having rise and fall times that do not exceed 0.4 microseconds.

Input Power (7.1) - The PAM decommutator is designed to operate with an input voltage of +22 to +37 volts.

Overvoltage (7.2) - See input power above.

Ripple (7.3) - The switching pre-regulator and the input filters allow normal operation with the specified ripple.

Undervoltage (7.4) - See input power above.

Transient Susceptibility (7.5) - The power supply was designed to withstand the specified transients. The tests showed no effect from the positive transients and only temporary loss of sync from the negative transients.

Feedback Ripply (7.6) - This was met by providing shunt regulation on the +6 volt supply and decoupling the power to the DAC power switch in addition to filtering in the power supply.

Reverse Polarity (7.7) - Reverse polarity protection is provided by a rectifier in series with the positive input lead.

Isolation (7.8) - dc isolation for ±100 volts between the primary power input and the signal outputs is provided by the converter transformer.

IV. PROBLEMS ENCOUNTERED AND SOLUTIONS

A. PHASE LOCK CIRCUITS

The original phase lock oscillator design was found to be satisfactory except when it was switched into and out of the HOLD mode. Two problems were discovered in relation to the HOLD mode. The first was when an uneven number of pulses were missing from the data train. An uneven number of missing pulses caused the divide by two flip-flop used to eliminate duty cycle effects to be in the opposite state from where it should be when the loop was switched from HOLD to TRACK. Then, when the loop drove to its desired condition, the address count was incorrect by one count. This condition was corrected by inserting a pulse from the PAM low counter into the divide-by-two flip flop after PAM had been at baseline for 0.875T and at T intervals thereafter until PAM again became high.

The second problem was that the loop drifted so much during the HOLD mode that it was out of sync at the end of the 10 missing pulses. The cause of this was that the integrator output voltage during HOLD was below its lowest ripple voltage due to the 0.875T delay after the last pulse received. This delay is necessary to avoid switching to the HOLD mode with a 70% duty cycle signal. This, when coupled with the high loop gain, caused the loop phase to be driven away from its last calculated phase. The solution to this, was to reduce the loop gain by reducing the gain of the integrator. This improved the situation from two standpoints in that not only was the phase not driven as far from nominal (i.e. the slope was not as steep) but also, since the ripple amplitude was decreased, the loop did not begin the HOLD mode as far from nominal. The necessary resistor value changes were made to obtain the nominal 92.16 KHz for A and B and 115.2 KHz for C and D.

B. SYNCHRONIZATION

The synchronization circuits, Figure IV-1, produced a number of minor problems. With the original circuitry, the set signal for the address counter was in error both by being too long and by improper phasing when the channel rate was above nominal. These problems were alleviated by using the event start signal, SE, and channel 1 to set the address counter (also see V.A.2).

A second problem was that the logic allowed a false sync condition where the address counter was in the channel 1 state and the PAM input was channel N (i.e. the last portion of the sync pulse). This was cured by resetting CH1 flip flop with $\overline{FP}$ and by resetting CHN flip flop with CH1 and CLA. Thus, if the circuit tries to get in the false sync condition, the following events will occur. Sync window, SW, will become true during n-1 instead of n period. This will set the CHN and frame sync reset (FSR) flip flops at the beginning of n-1. CH1 will set at the beginning of n and since FSR has not been reset by frame pulse, both SW1 and FSL will be reset. Note that CHN has not been reset due to CLA being low and since CH1 is true, the address counter has been set to address 1 by SE. At the

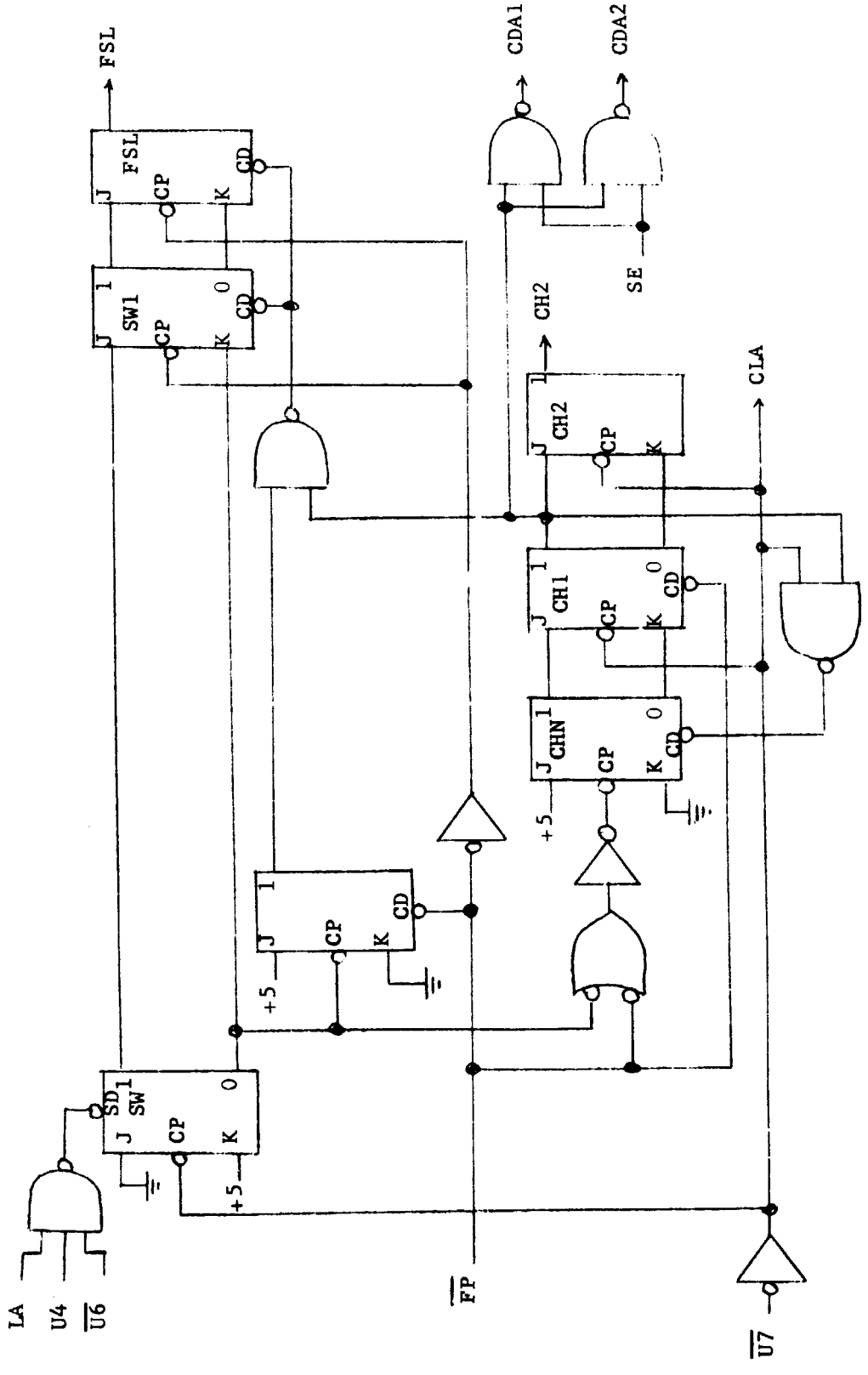

FIGURE IV-1, SYNCHRONIZATION CIRCUITS

0.25T point of channel n, the frame pulse is generated and $\overline{FP}$ clears CH1 and CHN continues to be true. Then, at the beginning of channel 1, CH1 is again clocked true since CHN is still true. The address register is again set to address 1 by SE and, at the middle of channel 1, CHN is cleared by CH1 and CLA. At this point, proper conditions exist for SW to occur during the next channel n (which allows SW1 to be set) and for a sync level indication, FSL, during the following channel n.

A possible hang up condition existed with the original circuit (where SW was clocked by $\overline{CH1}$) when SW was true and CHN was false. This turn-on condition blocked the CHN clock which prevented CHN from ever becoming true which, in turn, prevented CH1 from becoming true. Thus SW never received a falling clock and the circuit was locked up. The cure was simply to change the SW clock input from $\overline{CH1}$ to CLA.

A spike was found to occur on the last address, LA, line when the address counter was set to channel 1 address. This was a crossover spike that occurred only in format B because it has an uneven number of channels so that the least significant bit is true for both channel n and channel 1. This spike was eliminated by inserting the reset pulse, a logic zero signal, into the format B last address logic.

With a 70% duty cycle input signal, two start event signals were produced in format D. This occurred because the SE signal for format D is at count 15 and gating was not originally present to block a second pulse at count 79 or at the 62% point. The blocking signal was added by using an unused input of the inverter following the starting event OR circuit.

C. DATA CONDITIONING

In the original circuit design, the sample-and-hold circuit had a gain of one, but, early in the program this was increased to 1.5. Three circuit changes that should have been made at that time were made after fabrication. The 10K ohm $\pm$0.02% resistor should have been 15K ohm $\pm$0.02%. This was accomplished by inserting a series combination of 4.75K ohms and a 1K ohm potentiometer in series with the 1K ohm resistor. The potentiometer was one that had to be removed from the 100% reference amplifier - see section D. Also, the data level comparator resistors had to be changed to reflect the increased gain.

The other change required in the data conditioning was to reduce the gain of the differential dual gain input amplifier from 2 to 1.62 in the high gain state. This was necessary to accommodate a 2.5 volt peak-to-peak input signal that had a 2.5 volt baseline offset and a 30% zero reference. With a gain of 2, the sample-and-hold output voltage for the 0% reference was $[2.5 + 0.3\ (2.5)](1.5)2$ or 9.75 volts which is greater than the 8.5 volt reference. When the gain is reduced to 1.62 the voltage becomes $[2.5 + 0.3\ (2.5)](1.5)(1.62)$ or 7.9 volts which is well within the tolerance of the 8.5 volt reference.

D. DIGITIZER

Several small problems were encountered in the digitizer. The original clock signal to the digitizing register was high except during digitizing. However, the flip flops used in the register require the clock to be low when the direct set and clear inputs are used, so, to allow the 0% and 100% values to be set into the register and to allow direct clearing of the register, gating was added to provide a low clock except during digitizing.

The transfer pulse, TX, used to transfer the contents of the D register to the 0% and 100% storage registers was shortened to avoid a high clock condition for the least significant bit of those registers when the input to them was changing.

Several changes were made in the comparator circuitry to speed up the waveforms. However, since extreme speed is not of primary importance due to the way the sample-and-hold circuit is used, the digitizing clock was slowed to allow greater settling time for each approximation. These changes produced satisfactory performance.

The nulling pot originally used for the 100% reference amplifier was removed when it was found to produce a slight gain reduction in the amplifier. The gain reduction due to the nulling pot produced about a 20 millivolts drop on the output while the part spec lists the maximum offset without the pot as 5 millivolts.

E. MISCELLANEOUS

The DAC power switch produced several problems. It was originally included to reduce the average power consumption by turning off the ladder network switch drivers except during digitizing and to avoid connecting this heavy load to the full scale reference. The original switch amplifier was powered from +15 volts and ground. However, it was found that to avoid drawing the 6 ma per stage for the switch drivers, their supply voltage had to be reduced to less than a few tenths of a volt above their negative supply of -15 volts. So, the DAC power switch amplifier power supply was changed to $\pm$15 volts, two diodes were added to its input circuit to ensure a -15 volt input, and a diode was added in series with the -15 volt supply to the switch drivers. These changes effectively cut off the current drawn by the switch drivers.

A secondary effect of power switching is to produce ripple current on the PAM decommutator's power input. The ripple current amplitude was reduced by decoupling the +15 volt source for the power switch and by adding an additional 27 mfd filter capacitor from +15 volts to ground on the board containing the power switch.

The +6 volt supply was changed to shunt load regulation to avoid having to restrict the digital output loads to a very narrow range. Without the shunt regulator, the restriction would have been necessary to meet the input ripple current specification.

During EMI testing, several points between 25 MHz and 50 MHz were 10 and 15 db above the specification limits for radiated interference. A parasitic oscillation in the amplifier supplying bias to the computer input buffers was found to be the source of the signals. A 220 μf capacitor from the + input to ground stopped the oscillation.

V. RECOMMENDATIONS AND CONCLUSIONS

A. RECOMMENDATIONS

1. Data Ready Flag - The present circuit does not reset the data ready flag when data from a new address is requested. It does, of course, reset the data ready flag when data accept is received. The changes shown in Figure V-1 will add reset to the data ready flag for a data request pulse.

2. Synchronization - The present circuit used to provide frame sync level does not indicate sync when the channel rate is close to its upper extreme variation. This is due to the sync window flip flop, SW, being set after the frame sync pulse is generated and so 0's are transferred thru SW1 and FSL. This is because the gate used to avoid decoding spikes on the SW direct set uses U4 and $\overline{U6}$. In addition, it appears that in format D that sync may be lost due to the early occurrence of SE which is used to generate the address set signal for channel 1. As shown in Figure V-2, CLA can be used instead of U4 and $\overline{U6}$ to the set circuit for SW and the output of the digitizing time test point gate can be used instead of SE to set the address register. Neither change negates the original circuit operation. CLA will avoid spike problems since LA decodes the address register which is driven by the fall of CLA and so CLA is never high when the address counter is changing states. The digitizing time signal has the same characteristic of always occurring before transfer of data and addresses but it is always between the 0.25T point and the transfer. Thus it is more desirable than SE for use in this circuit.

3. DAC Power Switch - With the changes required to obtain proper operation using the power switch, the power savings originally anticipated were not obtained. In addition, even with the changes, the input ripple current is at the allowable maximum. Further investigation of the power switch circuitry and its use should be made.

4. Additional Units - In the event a second unit is desired, there are two methods of fabrication that can be used. The first is to essentially duplicate the present unit with jumper wires on the multilayer boards and other similar modifications. The second method is to redesign to incorporate the changes. The advantage of the first method is lower cost and probably faster delivery due to the redesign effort (delivery may, however, not depend on the boards as much as on the procurement of qualified components). The advantage of the second method is a much cleaner design. With either method but more particularly the second, the changes outlined in 1, 2 and 3 above should be evaluated and incorporated into the prototype if possible.

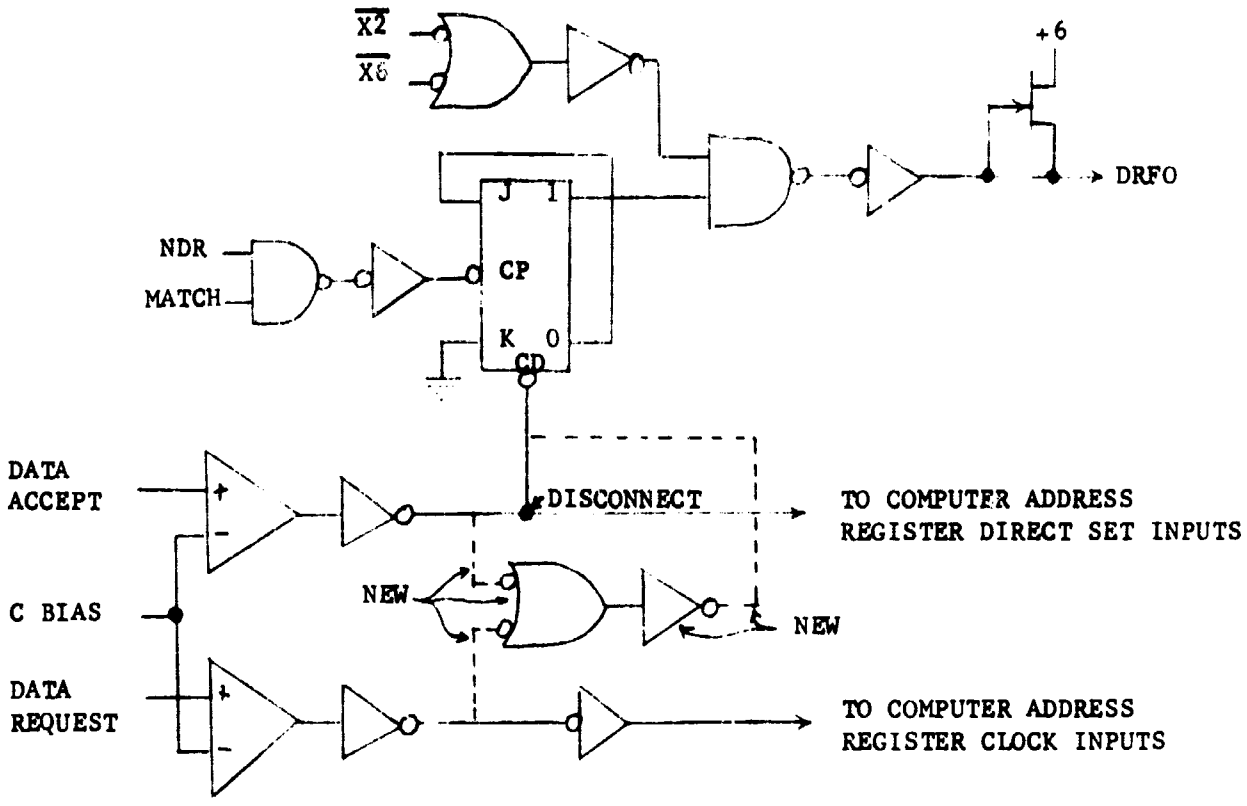

FIGURE V-1, DATA READY FLAG CIRCUIT

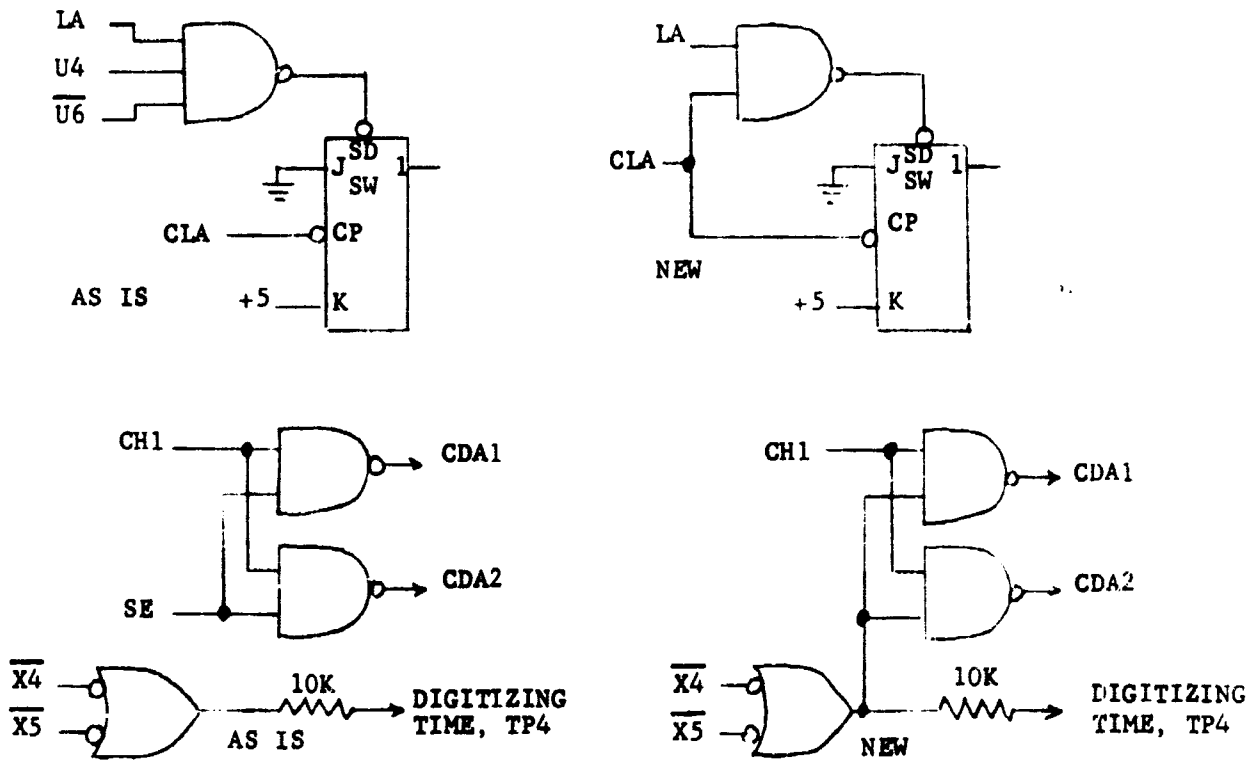

FIGURE V-2, ADDRESS COUNTER SET CIRCUIT

B. CONCLUSIONS

The prototype spacecraft microminiature PAM decommutator system designed, fabricated and tested under this contract meets the operational requirements of Exhibit A of the contract. However, the changes listed in Section A above will give improved performance. It is felt that the prototype also meets the intent of the specifications and will perform the final intended functions.

Both the electronic and mechanical designs appear to be good as evidenced by the facts that the PAM decommutators operation was affected very little by the environments to which it was subjected, and that the final weight was 46.3 ounces as compared with the required maximum of 50 ounces.

With the restriction of using only standard and, in some cases, selected components obtainable from reliable manufacturers, the packaging density of the PAM decommutator is very good. Any further reduction in size and weight using the same or similar components would require a much greater effort than that expended and would not be cost effective. To obtain any significant reduction in size and weight beyond that obtained would require procurement of components specifically designed for the unit and using the latest techniques for large scale integrated circuits. This would be quite costly and time consuming.

VI. TEST PROCEDURES AND DATA

The test procedure is detailed in MCR-69-135, Final Acceptance Test Procedure for Spacecraft Microminiature PAM Decommutator System, March 1969 as revised in July 1969.

The test data is included in the data package delivered with the unit and is summarized in MCR-69-370, Test Report for Spacecraft Microminiature PAM Decommutator System, July 1969.